

CLAIMS

1. A circuit for analyzing code coverage of firmware by test inputs, said circuit comprising:

an input for receiving an address from a code address bus;

a memory for storing recorded addresses from the code address bus, the memory comprising a plurality of memory locations, each of the memory locations mapped to a particular one of a corresponding plurality of addresses associated with the firmware; and

the contents of the memory location associated with the address received from the code address bus being incremented responsive to receipt of the address.

2. The circuit of claim 1, further comprising:

an address multiplexer for making a selection between the input and an address counter, and for providing the selection to the memory.

3. The circuit of claim 2, further comprising:

a data multiplexer for making a selection between an increment signal and a clear signal, and for providing the selection to the memory.

4. The circuit of claim 3, wherein if the data multiplexer selects the clear signal, and if the address multiplexer selects the address counter, then a memory location mapped to an address provided from the address counter is cleared.

5. A method for analyzing code coverage, said method comprising:

receiving an address from a code address bus, the address associated with an instruction in a system on chip; and

incrementing a memory location mapped to the address associated with the instruction.

6. The method of claim 5, further comprising:

selecting between the input and an address counter; and

providing the selection to the memory.

7. The method of claim 6, further comprising:

selecting between an increment signal and a clear signal; and

providing the selection to the memory.

8. The method of claim 7, wherein if the data the clear signal is selected, and the address counter is selected, then clearing a memory location mapped to an address provided from the address counter.

9. A circuit for analyzing code coverage of firmware by test inputs, said circuit comprising:

an input for receiving an address from a code address bus;

a memory operably connected to the input for storing recorded addresses from the code address bus, the memory comprising a plurality of memory locations, each of the memory locations mapped to a particular one of a corresponding plurality of addresses associated with the firmware; and

the contents of the memory location associated with the address received from the code address bus being incremented responsive to receipt of the address.

10. The circuit of claim 9, further comprising:

an address multiplexer connected to the input and an address counter, the multiplexer making a selection between the input and an address counter, and providing the selection to the memory.

11. The circuit of claim 10, further comprising:

a data multiplexer connected to the memory, the data multiplexer selecting between an increment signal and a clear signal, and providing the selection to the memory.

12. The circuit of claim 11, wherein if the data multiplexer selects the clear signal, and if the address multiplexer selects the address counter, then a memory location mapped to an address provided from the address counter is cleared.